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Design and Implementation of Digital Down-Converter for Wimax System

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Abstract: this paper presents the design and FPGA implementation for a digital down converter for a WiMax Communication system. Multistage implementation approach has been used to reduce the hardware requirement. The results have been presented for a Xilinx xc3sd1800a-4fg676 FPGA device.

Keywords: WiMax, Digital Communication, DDC

I. INTRODUCTION

Digital communication refers to the transmission of information using discrete messages. There are noteworthy advantages of transmitting data using discrete messages. It allows for enhanced signal processing and quality control for example errors caused by noise and interference can be detected and corrected systematically. A typical digital communication system can be represented as given in Figure 1.

Figure 1 Basic block diagram of digital communication system

The input block contains the source, which produces data and it also includes all the operations that are required to convert the original signal waveform into a format suitable for transmission. The transmitter takes bits from the input block and sends them over a channel. Communication channels can be of different types. For example, a transmission can take place over an Ethernet cable, a coaxial cable, or free space. The role of the receiver is to recover the original message from the received signal. This unit requires extra circuitry to extract the signal from noise and to correct errors that may have occurred during transmission. Finally, the output block takes the received information and puts it back into a format that is appropriate for the end-users.

A communication system uses multirate filters in several ways. Multirate processing finds application in shaping filters, in channelizers, in interpolators, in efficient bandwidth and sample rate reduction schemes, in anti-alias filtering, and in many other applications. A radio receiver down converts and demodulates a narrowband radio frequency (RF) signal embedded in a block of frequencies assigned to a particular radio service Yun Zhao et al.[2].

To control the computational workload, the filtering and down sampling is usually performed in multi stages. Figure 2 shows a multistage Digital Down converter (DDC) for a Wimax system T.K.Shahana et al [3]. The sampling rate is downconverted from the oversampled rate of sigma-delta modulator to a data rate that can be conveniently processed by existing DSP processors. This minimizes the power consumption of DSP processors for demodulation and equalization. The purpose of decimation filter is to remove all the out-of-band signals and noise, and to reduce the sampling rate from oversampled frequency of the sigma-delta modulator to Nyquist rate of the channel. The decimation filter consists of a lowpass filter and a downsampler. It is possible to perform noise removal and downconversion with a single stage finite impulse response (FIR) filter.

The power consumption of the filter depends on the number of taps as well as the rate at which it operates. So computational complexity is high for single stage implementation of decimation filter and consumes much power. This can be overcome by multi stage approach. Implementing decimation filter In several stages reduces the total number of filter coefficients. The filters operating at higher sampling rates have larger transition bands, and the filters with lower transition bands operate at reduced sampling frequencies. Subsequently, the hardware complexity and computational effort are reduced in multistage approach. This will lead to low power consumption. A multi stage sampling rate conversion (SRC) system consists of a cascade of single stage SRC systems as shown in Figure 2.

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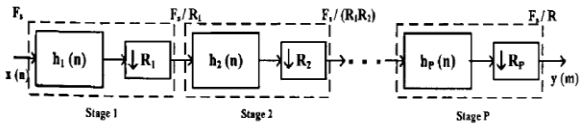

Figure 2 Block Diagram of a Multistage DDC for a Wimax system [3]

The proposed work is focused on design of digital down converter..

Using hardware system to perform these DSP tasks is a competent solution to this problem. FPGAs are often used as coprocessors to perform all the high speed tasks that cannot be achieved by microprocessors. FPGAs are chosen because they are on-site programmable and are highly suitable for hardware implementations. The software solutions adapted by the microprocessors to implement trigonometric functions are computer intensive. They do not suit hardware platforms because they need complex Circuits to perform the mathematical operations. Hence hardware algorithms are adopted for the calculation of trigonometric functions

II. DIGITAL DOWN CONVERTER

The process of sampling rate reducing the sampling rate by a factor M is called decimation. Decimation is a process that transforms a discrete-time signal with sampling rate f_s to another discrete-time signal with new sampling rate f_s.

A decimator realizes a sampling rate conversion (down-sampling) by an integer factor M: $f_s = f_s/M$, by using only every Mth input signal sample in the output signal. The output signal is at a lower sampling rate, and thus has a lower bandwidth ($f_s/2$) than the input signal (f_s /2). To avoid aliasing and thus ensure correct reproduction of the signal spectrum in $f_s/2$, the input signal has to be low-pass filtered before sampling rate conversion.

The block diagram of a decimator and example spectra of input, intermediate, and output signal for a decimation factor M = 3 are shown in figure 3. Note the different scaling of the normalized frequency axis in the output signal spectrum.

The input sequence x(n) is passed through a low pass filter, characterized by the impulse response & a frequency response H(ω) which ideally satisfies the conditionby Proakis et al. [26]

$$H(\omega) = \begin{cases} 1, & |\omega| \le \pi / D \\ 0, & otherwise \end{cases} \qquad (1)$$

The output of the filter is a sequence u(n) given as by Proakis et al. [26]

$$v(n) = \sum_{k=0}^{\infty} h(k)x(n-k) \qquad (2)$$

which is then down sampled by factor M to produce y(m) by Proakis et al. [26]

$$y(m) = \sum_{k=0}^{\infty} h(k)x(mM-k) \qquad (3)$$

The frequency domain characteristics of the output sequence y(m) can be conveniently defined as by Proakis et al. [26]

$$\bar{v}(n) = \begin{cases} v(n), & n = 0, \pm M, \pm 2M ..... \\ 0, & otherwise \end{cases} \qquad (4)$$

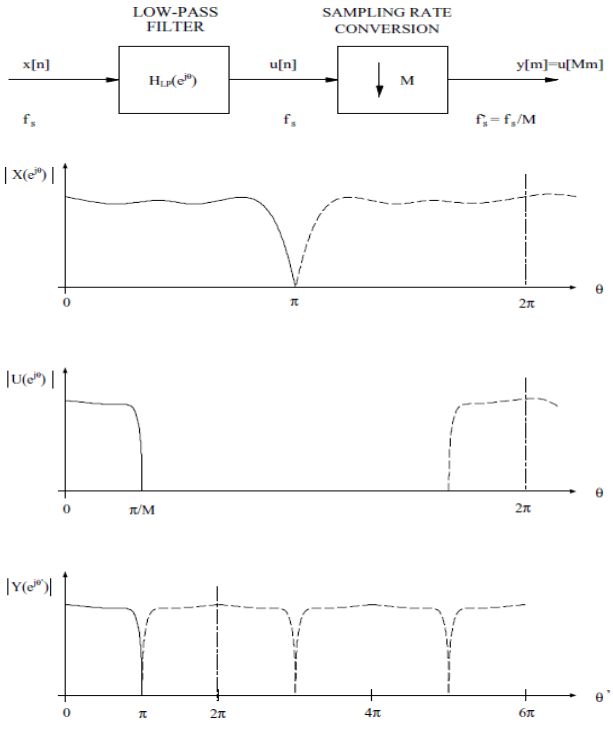

Figure 3 Spectral Characteristics of a decimator and example signal spectra for M=3by Proakis et al. [1]

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The final decimated output is given by by Proakis et al. [26]

$$y(m) = \frac{1}{M} H(\frac{\omega y}{M}) X(\frac{\omega y}{M}) \quad \text{for } 0 \le |\omega_y| \le \pi \qquad (5)$$

III. IMPLEMENTATION OF DIGITAL DOWN-CONVERTER

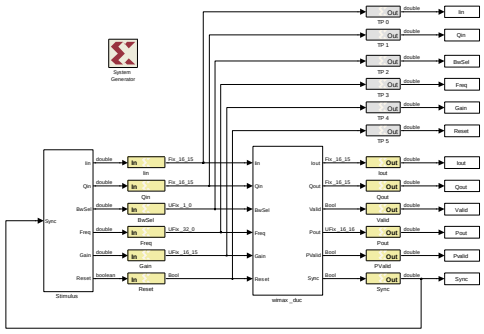

Figure 4 System Generator setup for DDC

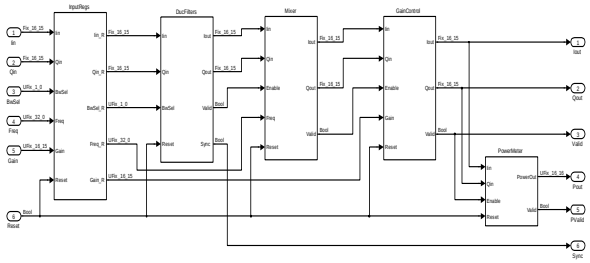

Figure 5 Internal View of System Generator setup for DDC

Figure 4 show the complete setup developed using system generator and Figure 5 shows the details of DDC module.

Table 1: Resources utilized by DDC Module

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	1651	16640	9%
Number of Slice Flip Flops	2923	33280	8%
Number of 4 input LUTs	1829	33280	5%
Number of bonded IOBs	178	519	34%
Number of BRAMs	2	84	2%
Number of GCLKs	1	24	4%
Number of DSP48s	21	84	25%

The setup shown in Figure 5 has been simulated and synthesized using ISE 9.2i software. Table 1 shows the resources used by the design for xc3sd1800a-4fg676 FPGA device.

From Table 1, it has been concluded that the proposed design uses only very small number of FPGA resources.

IV. CONCLUSION

DDC is in integral part of a digital communication receiver and its multistage design leads to the requirement of less number of FPGA resources. This paper shows the successful implementation of DDC for a WiMAX system. The resources utilized by the proposed design are well below the hardware utilization reported in previous works.

REFERENCES

1. J.G. Proakis and D.G. Manolakis, "Digital Signal Processing: Principles, Algorithms and Applications (3rd ed.)", New Delhi: PHI Publications Inc., 2006.
2. Wenmiao Song &BoLiu,"Design of the CIC decimation filter Based on SOPC Builder", 978-1-4244-5540-9/10/2010 IEEE.
3. Yun Zhao, Li Jun Wang, and Jian Liang Xu,"Implementation of Sample Rate Conversion in Direct RF Synthesis Transmitter", 2011 Cross Strait Quad-Regional Radio Science and Wireless Technology Conference 978-1-4244-9793-5/11/2011 IEEE.